JVC

SERVICE MANUAL

PORTABLE ROM PLAYER

XA-GP3BK

Area Suffix

E --- Continental Europe

This guidance system is a combination system configuration of XA-GT1TN, XA-GC20BK, and XA-GP3BK.

Contents

No.21034
Oct. 2001

Safety precaution

⚠ ***CAUTION*** **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Disassembly method

■ Detaching the bottom case from the unit

(Refer to Fig.1 to 3)

Be sure to eject the flash memory card from the unit before dismantling it. To eject the flash memory card, use a flat head screwdriver (diameter 2 mm) to press the round groove that can be seen when the power switch on the right side of the unit is set to "OFF" (Refer to Fig. 1)

1. Turn the unit upside down and detach the screw at A fixing the battery cover (Refer to Fig. 2)

2. Remove the rechargeable Lithium-ion battery from the unit (Refer to Fig. 3)

3. Remove the two screws at both B and C fixing the bottom case, then remove the bottom case from unit. (Refer to Fig. 3)

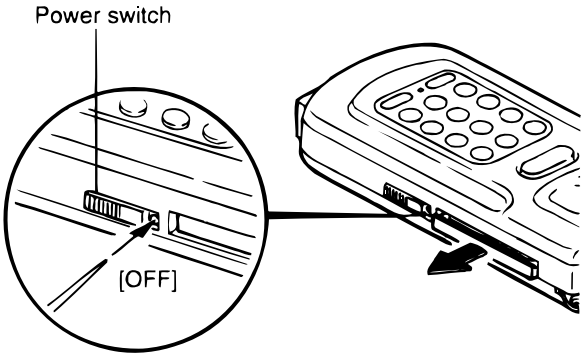


Fig. 1

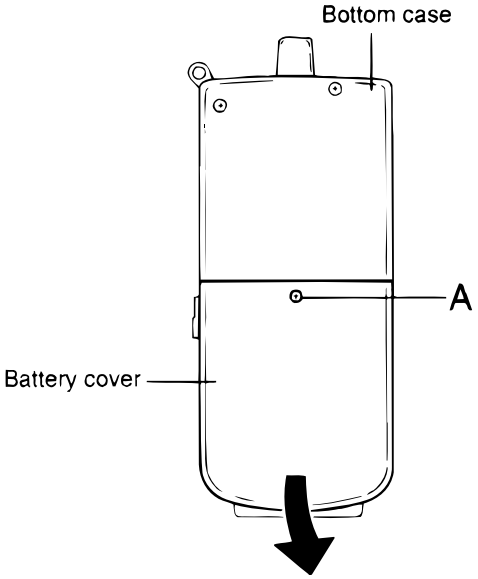


Fig. 2

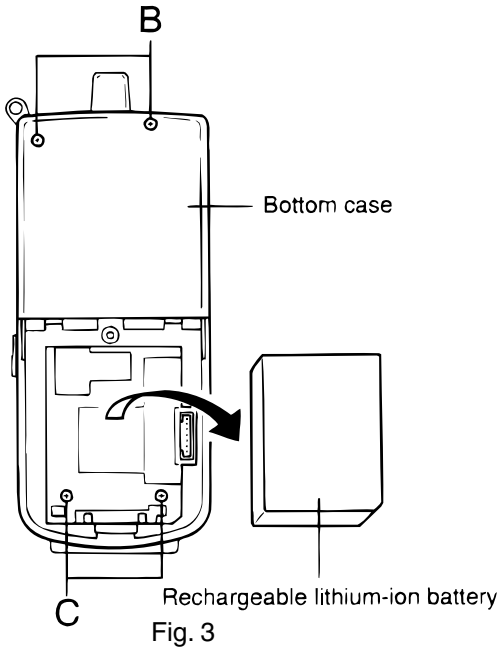


Fig. 3

■ Detaching the top case from the unit (Refer FIg.4 to 7)

1. Remove the bottom case.
2. Pull out the two pins and holder bracket fixing the center cover.
3. Pull the center cover outward to unhook the six joints at a and the two joints at b, and then slide the center cover upward to remove it from the unit.
4. Remove the screw at D fixing the infrared board (Refer to Fig. 6)
5. Unplug the infrared board connection cable from the CN301 connector on the main board. (Refer to Fig. 6)
6. Remove the two screws at E fexing the main board. (Refer to Fig.6)
7. Unhook the joint at C to detach the battery charging terminal unit from the top case ,then remove the main board from the top case.
8. If necessary, unplug the card wire from the CN102, and CN103 connectors on the main board (Refer to Fig.6)
9. Remove the two screws at F fixing the LCD module board . (Refer to Fig. 7)
10. Unplug the LCD module board connection cable from the CN203 connector on the key board, then remove the LCD module board. (Refer to Fig. 7)
11. Remove the five screws at G fixing the key board, then remove the key board. (Refer to Fig. 7)

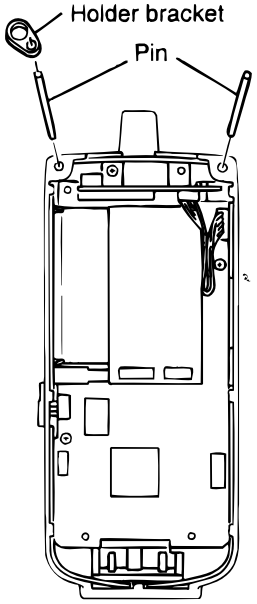


Fig. 4

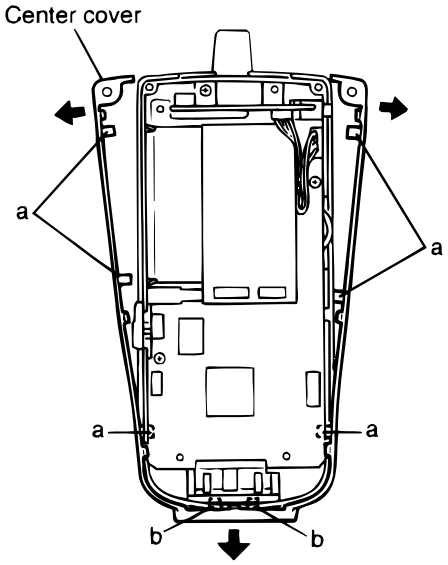


Fig. 5

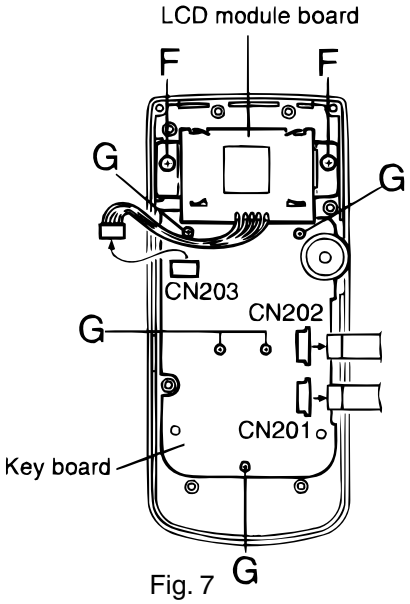


Fig. 7

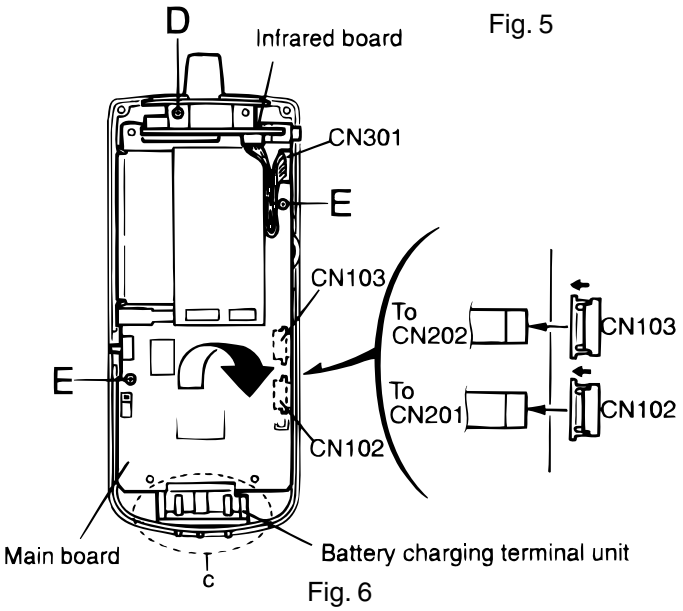


Fig. 6

Adjustment method

Measuring instructions
Distortion meter
AC voltage meter
DC voltage meter
Reference values for measuring
Power supply voltage --- DC3.7V ±0.1V
Playback gain --- -7.0dB ±2dB (Measured at the headphone terminal by circuit A when the volume is at maximum and ROM card No. 103 is playback)

--- -55dB ±3dB (When the volume is at minimum under the same condition as above.)

High frequency distortion ---Less than 0.3%/THD (measured at the headphone terminal by circuit A when the volume is at maximum and ROM card No. 103 is playback)

S/N ratio ---- More than 70dB (The Difference in output measured at the headphone terminal by circuit A when the volume is at maximum and ROM card No. 103 and No.130 are playback)

Channel separation ---- More than 45dB (Sound leakage in the reverse side of the headphone terminal measured by circuit A when ROM card No.120 and No.121 are playback)

Frequency characteristics	1kHz Standard range (File No. 103)	
44.1kHz sampling	63Hz -3.0dB ±3dB (File No. 100)	
	15kHz-3.0dB ±3dB (File No. 108)	The frequency should be within the above listed standard range against 1 kHz when each file is playback .use circuit A for measuring
	315Hz 0dB ±2dB (File No. 110)	
22.05kHz sampling	1kHz 0dB ±1dB (File No. 111)	
	6.3kHz -0.5dB ±2dB (File No. 112)	
	315Hz 0dB ±2dB (File No. 115)	
16.0kHz sampling	1kHz 0dB ±1dB (File No. 116)	
	6.3kHz -11.5dB ±3dB (File No. 117)	

Power consumption	PLAYBACK DC 110mA ±20mA	
	STOP DC 1mA ±2mA	Set the unit to the test mode
	SLEEP DC 5mA ±3mA	Use circuit B for measuring.
	DEEP SLEEP DC Less than 200μA	
	POWER OFF DC 0mA	

Optical characteristics (light reception range) ----More than 4m

Within the standard distance that can receive output from the XA-GT1(14.82mW/sr).

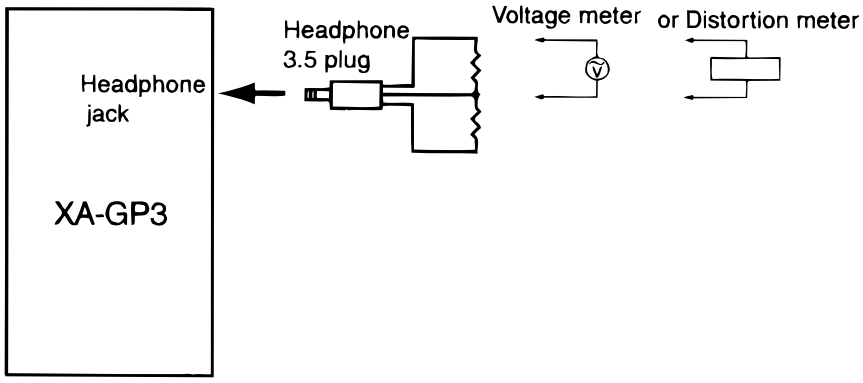
ROM file No.

File No. 103	1kHz standard signal
File No. 120	L-R for confirming cross talk
File No. 121	R-L for confirming cross talk
File No. 100	63Hz for confirming F-special measuring signal
File No. 108	15Hz for confirming F-special measuring signal
File No. 110	315Hz for confirming F-special measuring signal
File No. 111	1kHz for confirming F-special measuring signal
File No. 112	6.3kHz for confirming F-special measuring signal
File No. 115	315Hz for confirming F-special measuring signal
File No. 116	1kHz for confirming F-special measuring signal
File No. 117	6.3Hz for confirming F-special measuring signal
File No. 000	1kHz for confirming power consumption

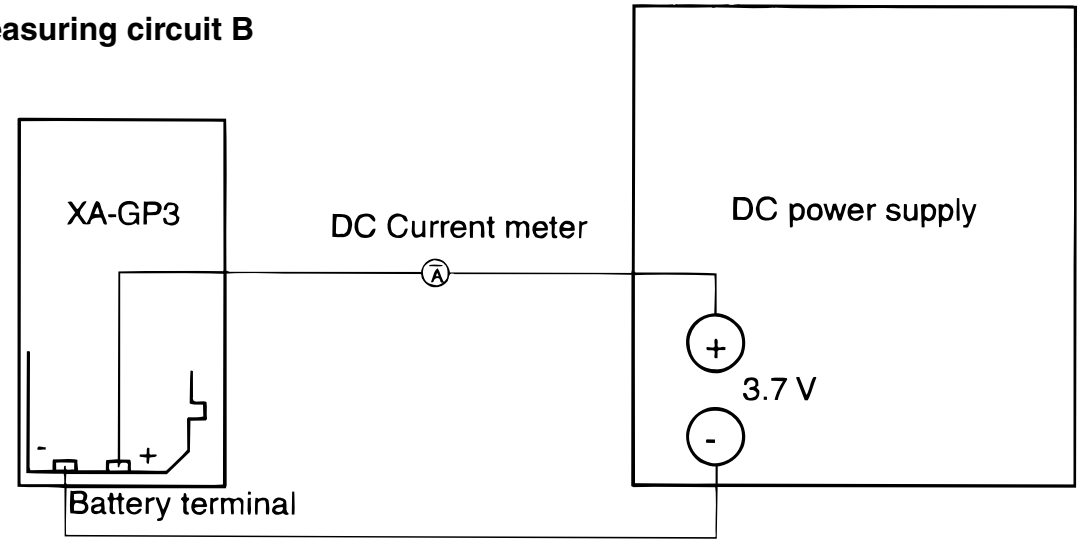
<Note>
The XA-GP3 is not compatible with the recording system of the XA-GP1's ROM card as it uses a different type of recording system.
The amount of space in the XA-GP3's ROM card is also much greater to allow it to store a large amount of data.

<How to set the unit to the test mode>
Turn the power on while pressing start key and "1"key.
When in the test mode, press the start key to go to the next step.

Measuring circuit A



Measuring circuit B



Set the unit to the test mode for measuring.

Setting the test mode on the XA-GP3

Setting the test mode
Insert the TEST card into the unit.
Turn the power on while pressing the start key and "1 " key on the unit.
The software's version number appears on the LCD monitor. (eg: d1 .0)
Press the start key on the unit to go to the next step.

1. Digital circuitry test
The test stops if an error occurs during the test mode. If this happens, it will restart and go to the next step when the start key on the unit is pressed. If a CF card is not loaded in the unit, "nCF" will appear and the test will be aborted when the CF card read test is performed. The test will restart and go to the next step when the start key on the unit is pressed.

2. LCD monitor display test
Each segment on the LCD monitor.flashes every 200 microseconds. At this time, the LED (light emiting diode) will blink on the LCD monitor. Press the start key on the unit to go to the next step.

3. Battery voltage detection test
The LCD monitor displays the AD value converted to the decimal system every 500 microseconds. Press the start key on the unit to go to the next step.

4. Power consumption test (Perform the above three tests first.)
The five modes listed below need to be tested.

o PLAYBACK
"_PB" appears on the LCD monitor. At this time, File No.. 000 is played back if it is in the CF card. If not, "nFL" appears on the LCD monitor. If a CF card is not loaded in the unit, "nCF" appears on the LCD monitor.

o STOP
"_SP" appears on the LCD monitor. Press the start key on the unit to go to the next step.

o SLEEP MODE
"_SL" appears on the LCD monitor. Press the start key on the unit to go to the next step.

o DEEP SLEEP MODE
"dSL" appears on the LCD monitor. Press the start key on the unit to go to the next step.

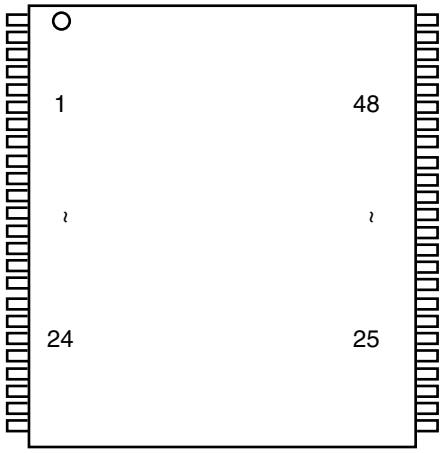
o RESET
Press the start key. "RES" appears on the LCD monitor.

Finishing the test mode
Turn the unit's power off.

Description of major ICs

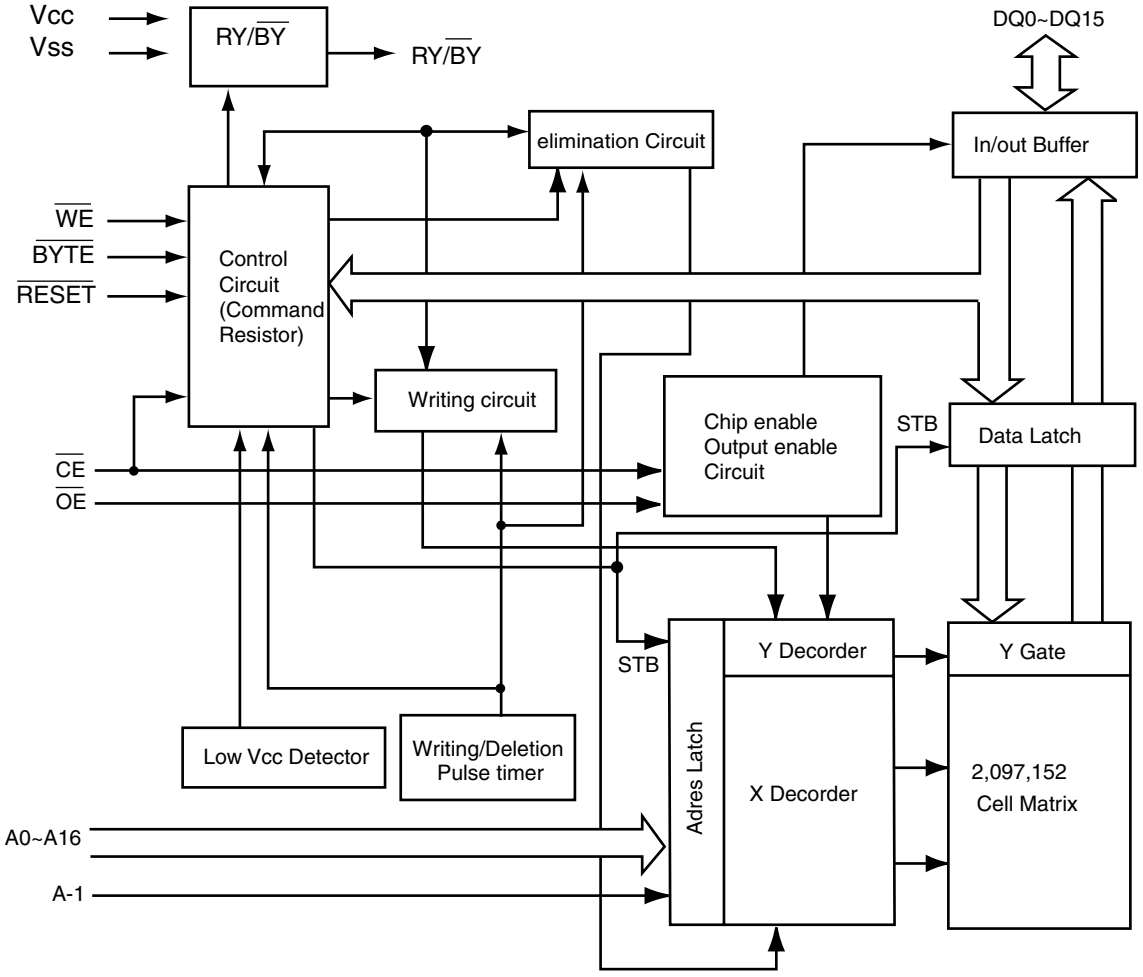
■ MBM29LV2BC9TN (IC105) : Cord frushe

1. Pin layout



(TOP VIEW)

2. Block diagram

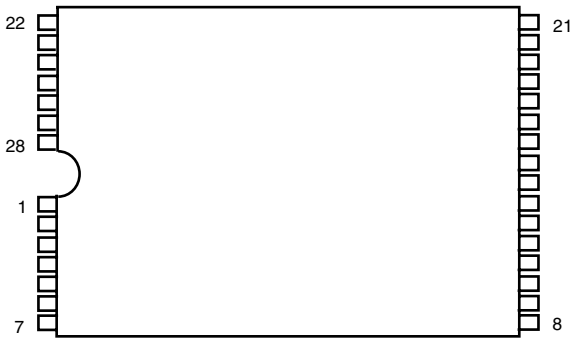


3.Pin function

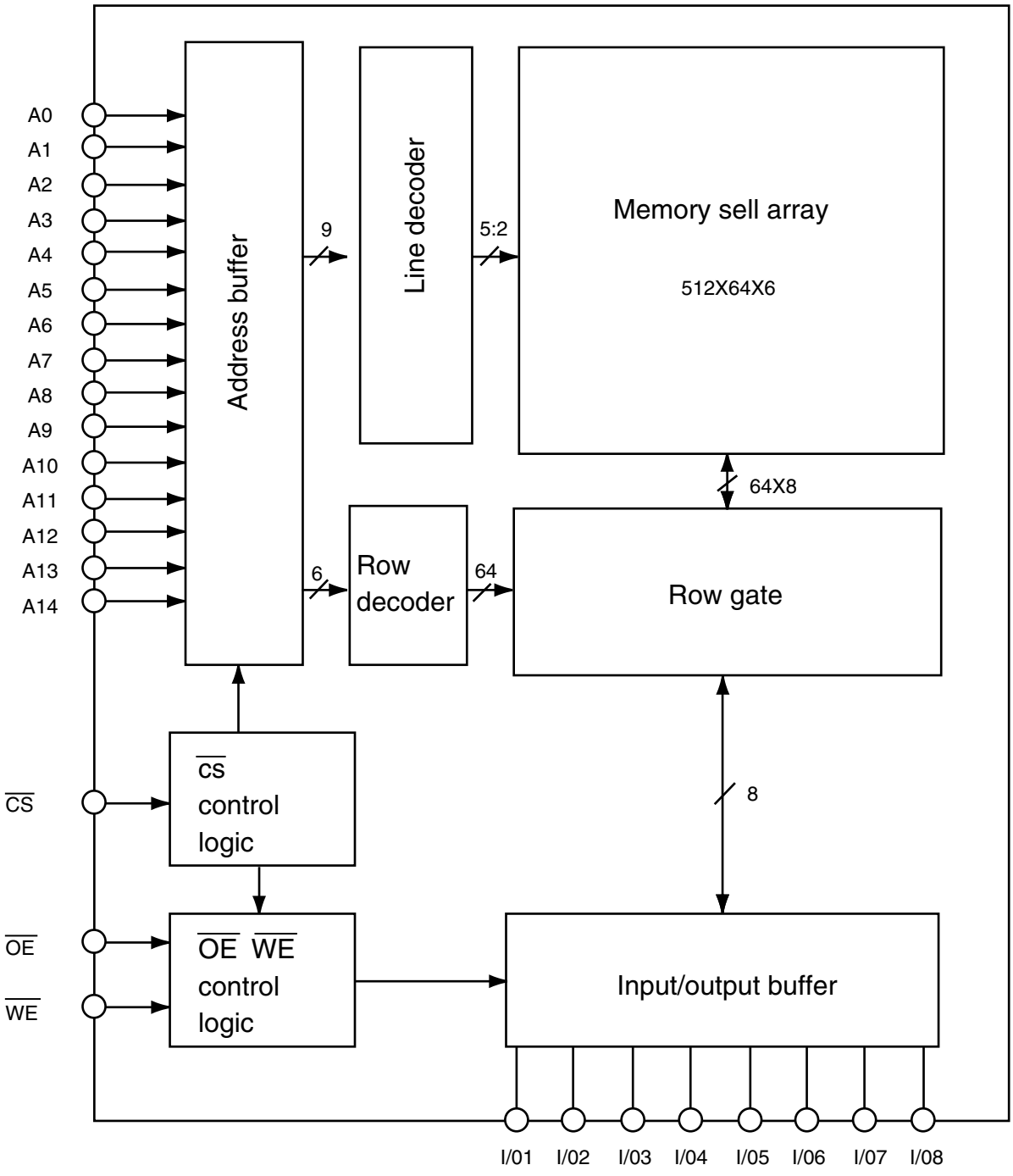
Pin No.	Symbol	Function
1	A15	Input address
2	A14	
3	A13	
4	A12	
5	A11	
6	A10	
7	A9	
8	A8	
9	N.C	Non connection
10	N.C	
11	/WE	Writ enable
12	/RESET	Hardware reset
13	N.C	Non connection
14	N.C	
15	RY/BY	Ready and busy output
16	N.C	Non connection
17	N.C	
18	A7	Address input
19	A6	
20	A5	
21	A4	
22	A3	
23	A2	
24	A1	
25	A0	
26	/CE	Chip enable
27	Vss	GND
28	/OE	Output enable
29	DQ0	Data in / out
30	DQ8	
31	DQ1	
32	DQ9	
33	DQ2	
34	DQ10	
35	DQ3	
36	DQ11	
37	Vcc	Power supply
38	DQ4	Data in / out
39	DQ12	
40	DQ5	
41	DQ13	
42	DQ6	
43	DQ14	
44	DQ7	
45	DQ15	
46	Vss	GND
47	/BYTE	8bit and 16bit mode select
48	A16	Address input

■SRM2B256SLTMX5 (IC106) : SRAM

1. Pin layout



2. Block diagram

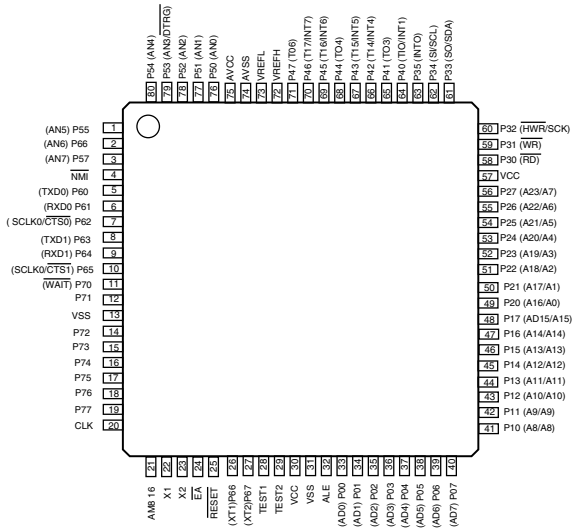


3.Pin function

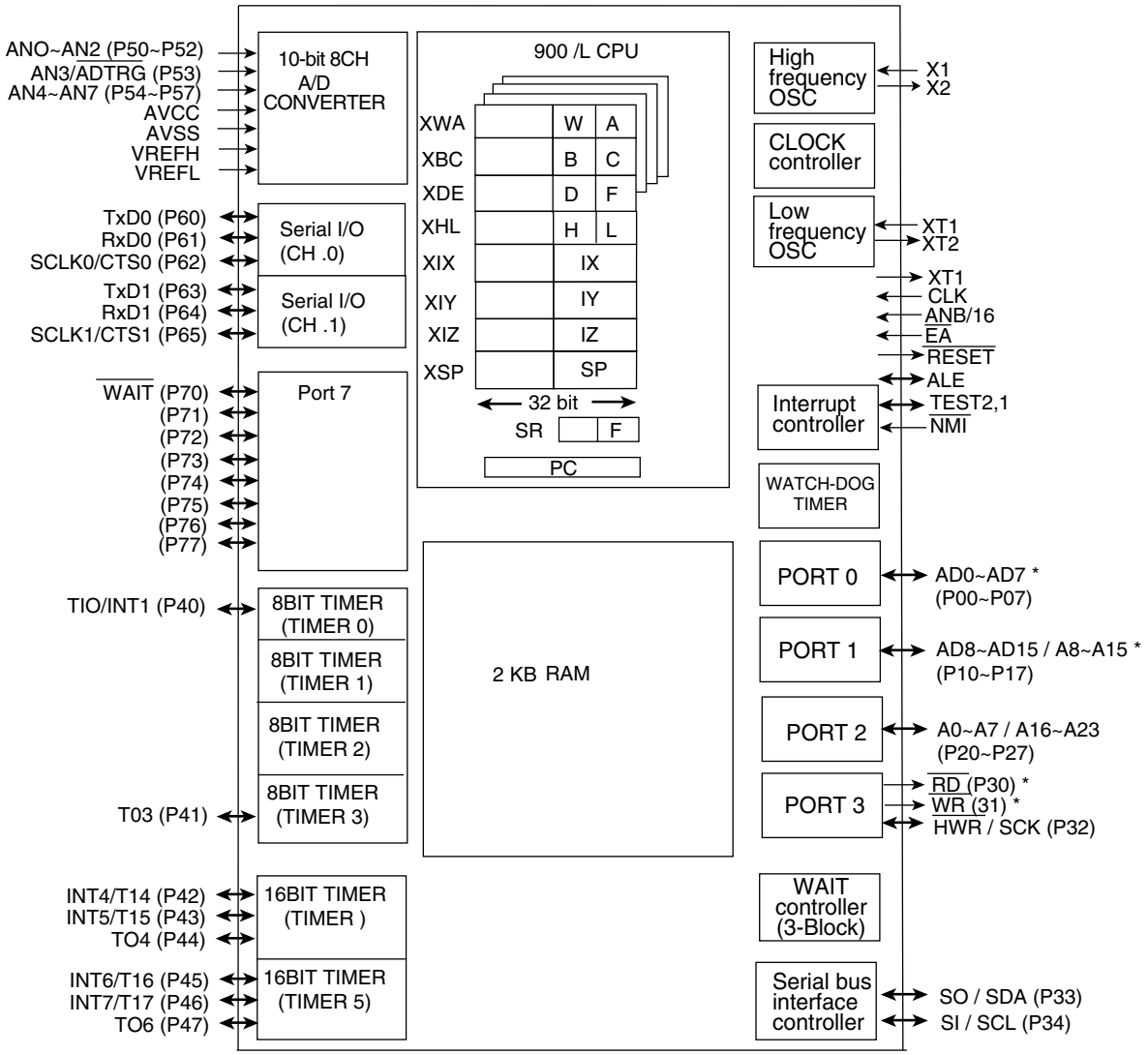
Pin No.	Symbol	Function
1	A15	Input address
2	A14	
3	A13	
4	A12	
5	A11	
6	A10	
7	A9	
8	A8	
9	N.C	Non connection
10	N.C	
11	/WE	Writ enable
12	/RESET	Hardware reset
13	N.C	Non connection
14	N.C	
15	RY/BY	Ready and busy output
16	N.C	Non connection
17	N.C	
18	A7	Address input
19	A6	
20	A5	
21	A4	
22	A3	
23	A2	
24	A1	
25	A0	
26	/CE	Chip enable
27	Vss	GND
28	/OE	Output enable
29	DQ0	Data in / out
30	DQ8	
31	DQ1	
32	DQ9	
33	DQ2	
34	DQ10	
35	DQ3	
36	DQ11	
37	Vcc	Power supply
38	DQ4	Data in / out
39	DQ12	
40	DQ5	
41	DQ13	
42	DQ6	
43	DQ14	
44	DQ7	
45	DQ15	
46	Vss	GND
47	/BYTE	8bit and 16bit mode select
48	A16	Address input

■ TMP93CS45F (IC101) : 16Bit CPU

1.Pin layout



2.Block diagram



Note : The pin state after reset

Product name	AM8 / 16	Pin function after reset
TMP93CS45	AN3	Except" pins,item in parentheses ( ) are the initial setting after reset.
	AN4	Except" pins,item in parentheses ( ) are the initial setting after reset. However,port 1 is initialized item of parentheses.

3.Pin function (1/2)

TMP93CS45F (1/2)

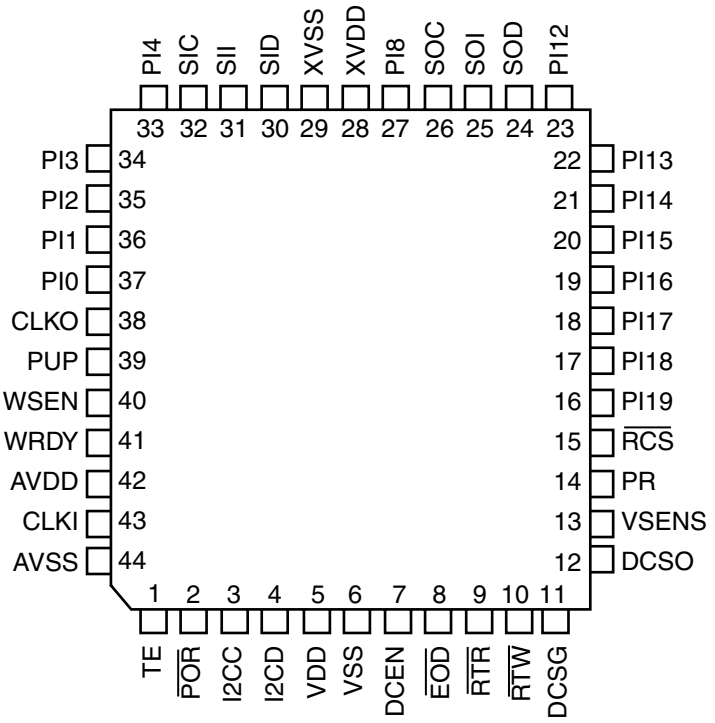
Pin No.	Symbol	I/O	Function
1 2 3	P55 P56 P57	I	Port 50 - 52, 54 - 57 : For input only.
4	NMI	I	Non-maskable interrupt request terminal: Makes the boot-up edge and falling edge programmable.
5	TXD0	O	Serial transmit data 0.
6	RXD0	I	Serial receive data 1.
7	SCLK0	O	Serial clock IN/OUT 0.
8	TXD1	O	Serial transmit data 1.
9	RXD1	I	Serial receive data 1.
10	P65	O	Port 65: IN/OUT port (with built-in pull-up resistance).
11	P70	O	Port 70: IN/OUT port (can drive a large amount of current).
12	P71	O	Port 71 - 77: IN/OUT port that enables IN/OUT setting in bits. (can drive a large amount of current).
13	VSS	I	Ground terminal (connect all VSS terminals to GND (0 V)).
14 15 16 17 18 19	P72 P73 P74 P75 P76 P77	O	Port 71 - 77: IN/OUT port that enables IN/OUT setting in bits (can drive a large amount of current).
20	CLK	O	Clock output: Outputs the clock with f SYS divided into two. Pulled up during a hard reset. (Can be set not to output to reduce noise.)
21	AM8/16	I	Address mode: Terminal for selecting the width of the external data bus. Connect to GND when using a 16-bit external bus or 8/16-bit external bus. Connect to VCC when using an 8-bit terminal.
22	X1	I	High-frequency oscillator connection terminal.
23	X2	O	High-frequency oscillator connection terminal.
24	EA	I	External access: Connect to GND.
25	REST	I	Hard reset for unitizing (with built-in pull-up resistance).
26	XT1	I	Low-frequency oscillator connection terminal.
27	XT2	O	Low-frequency oscillator connection terminal.
28 29	TEST1 TEST2	I/O	Test terminal (connect these terminal on the base).
30	VCC	I	Power supply terminal (connect these terminals on the base).
31	VSS	I	Ground terminal (connect all VSS terminals to GND (0 V)).
32	ALE	O	Address latch enable (Can be set not to output to reduce noise).
33 34 35 36 37 38 39 40	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	3 STATE	Address data (lower): Address/data bus 0 - 7.
41 42 43 44 45 46 47 48	AD8 AD9 AS10 AD11 AD12 AD13 AD14 AD15	3 STATE	Address data (higher): Address/data bus 8 - 15.

TMP93CS45F (2/2)

PIN No.	Symbol	I/O	Function
49 50 51 52 53 54 55	A16 A17 A18 A19 A20 A21 A22	O	Address: Address bus 16 - 23.
56	A23	O	Address: Address bus 16 - 23.
57	VCC	I	Power supply terminal (connect all VCC terminals to the power supply).
58	RD	O	Read: Outputs the strobe signal to read the external memory.
59	WR	O	Write: Outputs the strobe signal to write data to the AD 0 - 7 terminals.
60	HWR	O	Write higher: Outputs the strobe signal to write data to the AD 8 - 15 terminals.
61	SDA	I/O	Data IN/OUT terminal for the I2 C bus mode on the serial bus interface.
62	SCL	I/O	Clock IN/OUT terminal for the I2 C bus mode on the serial bus interface.
63	INT0	I	Interrupt request terminal 0: Makes the level and boot-up edge programmable.
64	P40	I	Port 40: Input port.
65	P41	I	Port 41: Input port.
66	INT4	I	Interrupt request terminal 4: Makes the boot-up edge and falling edge programmable.
67	INT5	I	Interrupt request terminal 5: Makes the boot-up edge programmable.
68	P44	I/O	Port 44: Input port.
69	INT6	I	Interrupt request terminal 6: Makes the boot-up edge and falling edge programmable.
70	INT7	I	Interrupt request terminal 7: Makes the boot-up edge programmable.
71	P47	O	Output port.
72	VREFH	I	Reference voltage input terminal for the A/D converter (high).
73	VREFL	I	Reference voltage input terminal for the A/D converter (low).
74	AVSS	I	Ground terminal (0 V) for the A/D converter.
75	AVCC	I	Power supply terminal (0 V) for the A/D converter.
76 77 78	AN0 AN1 AN2	I	Analog input 0 - 2, 4 - 7: Input terminal for the A/D converter.
79	AN3	I	Analog input 3: Input terminal for the A/D converter.
80	AN4	I	Analog input 0 - 2, 4 - 7: Input terminal for the A/D converter.

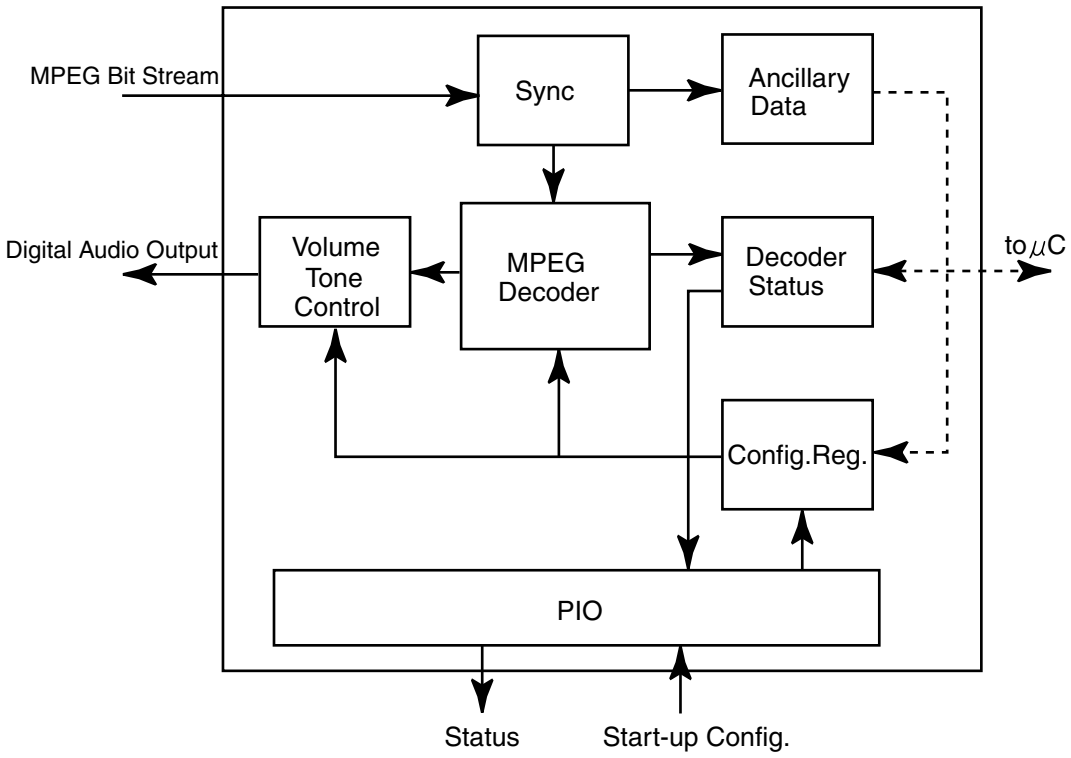
■MAS3507D (IC201) : MPEG decorder

1. pin layout



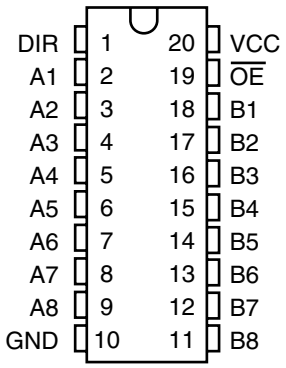
(TOP VIEW)

2. Block diagram

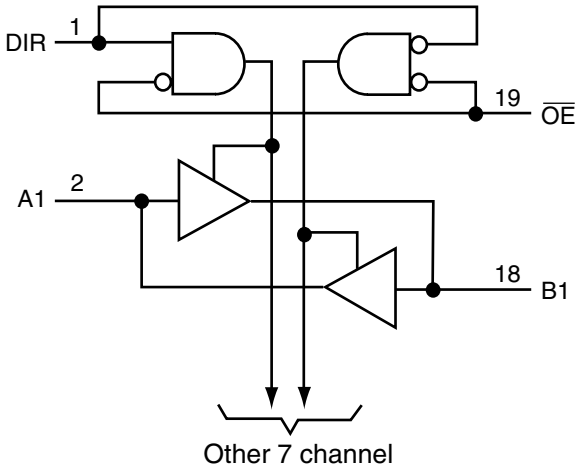


■ SN74LVCH245APWX (IC110,IC112,IC113) : 8bus circuit transceiver

1. pin layout



2. Block diagram



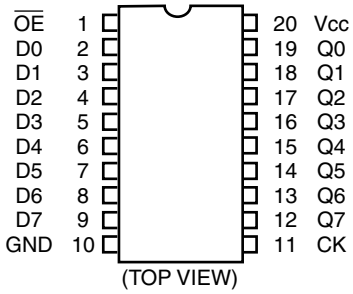
3. Pin function

Input		Functions
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

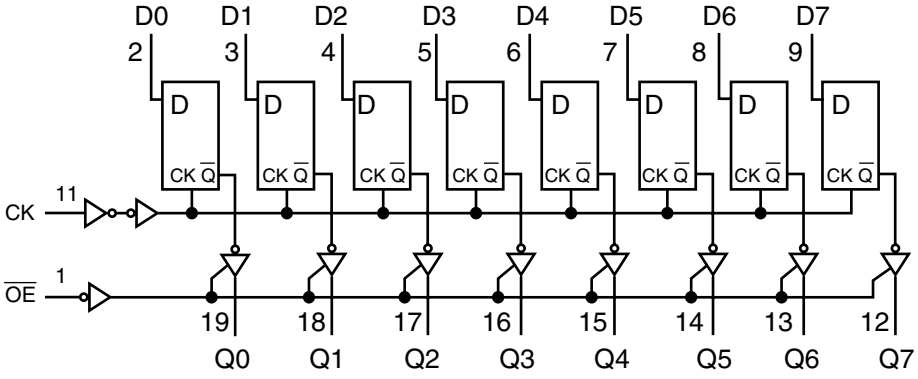
H : High level
L : Low level
X : No specification

■ TC74VHC574FT(IC103,IC104,IC108,IC109) : 8bit frip-flop

1. pin layout

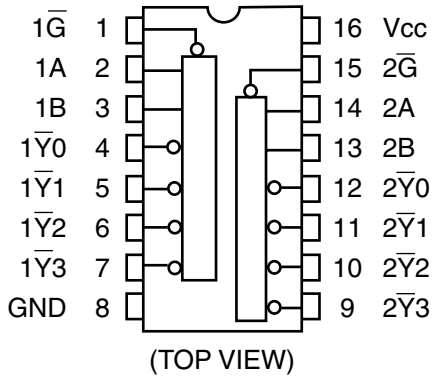


2. Block diagram

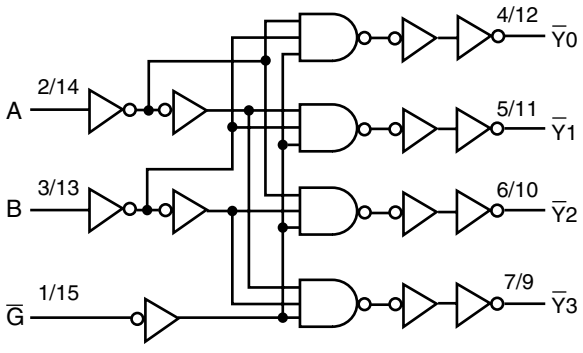


■ TC74VHC139FT (IC102) : Dual decoder

1. pin layout

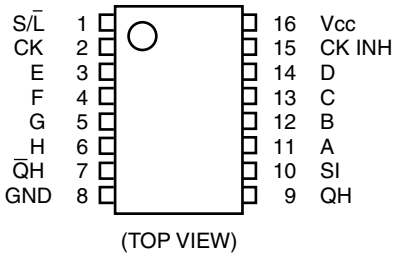


2. Block diagram



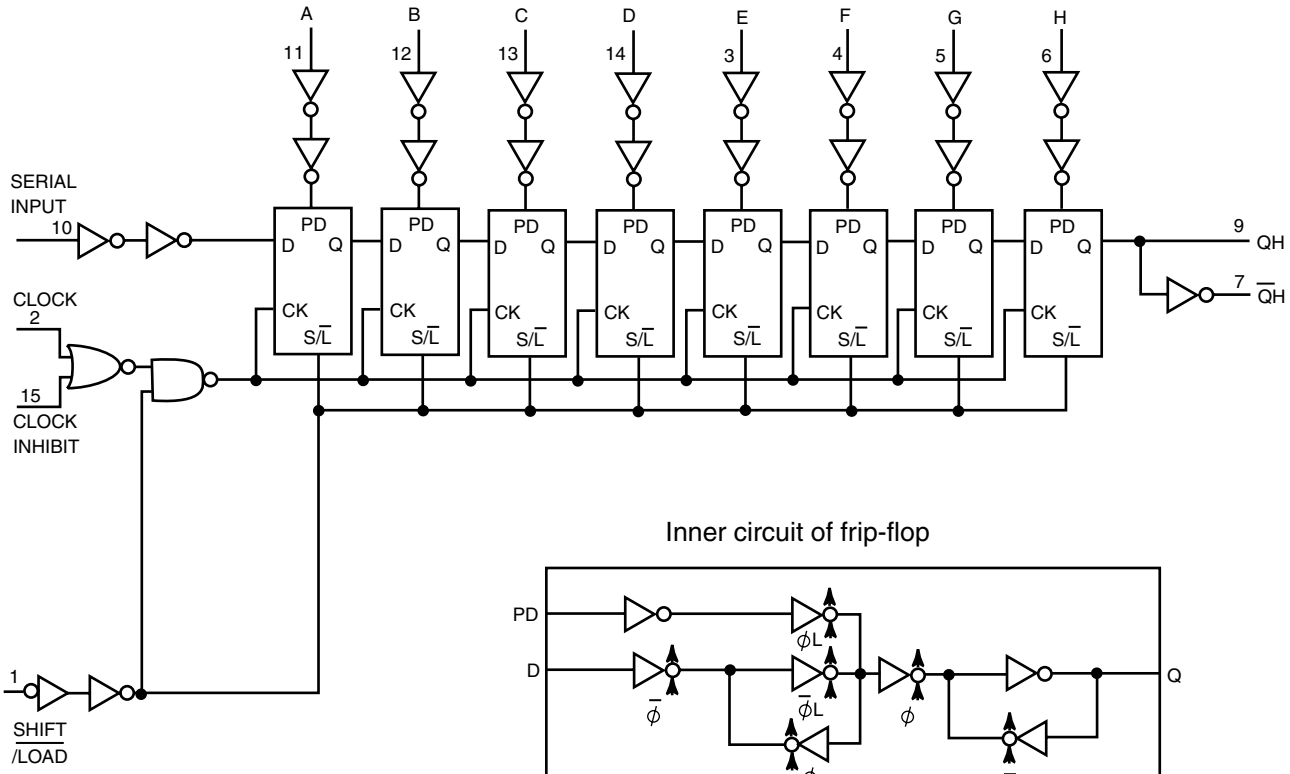
■ TC74VHC165FT (IC203) : 8bit shift resistor

1. Pin layout



(TOP VIEW)

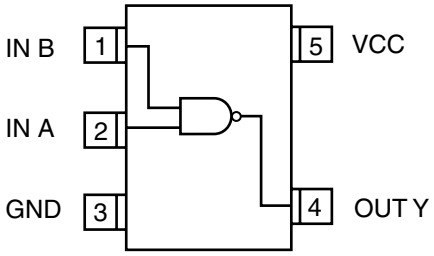
2. Block diagram



Inner circuit of frip-flop

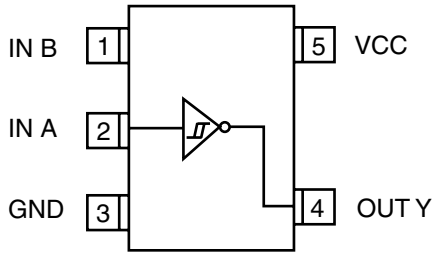
■ TC7SH04FU (IC107,IC113,IC116) : 4-NAND Gate

1. pin layout



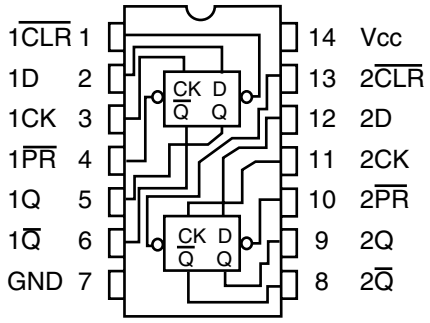
■ TC7SH14FU (IC205) : Schmitt trigger inverter

1. pin layout



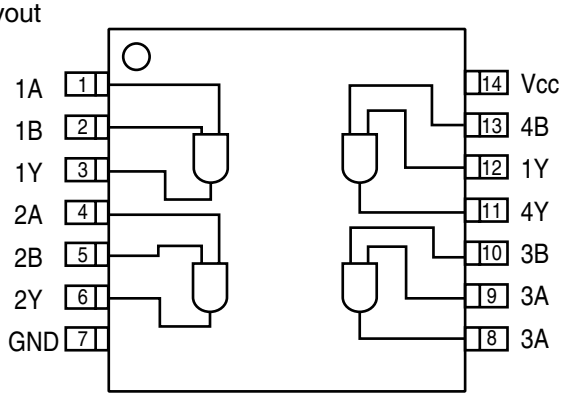
■ TC74VHC74FT (IC115) : Frip-flop

1. pin layout



■ TC74HCT08AFT (IC204) : 4-NAND Gate

1. pin layout



XA-GP3BK

JVC

VICTOR COMPANY OF JAPAN, LIMITED
AUDIO & COMMUNICATION BUSINESS DIVISION
PERSONAL & MOBILE NETWORK BUSINESS UNIT. 10-1,1chome,Ohwatari-machi,Maebashi-city,371-8543,Japan

(No.21034)

200110(V)